SPECIFICATION

Amend paragraph 33 of the specification as follows:

[0033] FIG. 2 illustrates an embodiment of controller 105. Controller 105 comprises an oscillator 140, which is preferably a high frequency oscillator, having for example, an 8MHz.CLK. Oscillator ~~108~~ 140 issues, through a divider, a 50ns pulse every 2μs (500kHz). This pulse is used to load into duty cycle generator 148 a numerical value stored in an up-down digital counter (memory) 146. The period generator 144 generates more finely divided clock from the oscillator (clock) ~~108~~ 140. The ratio of the oscillator clock frequency to the period generator clock frequency is equal to the number of levels for the duty cycle value. For example if the oscillator frequency is 8Mhz and period generator clock frequency is 500KHz, there would be 16 possible values for the duty cycle (8/0.5=16).